



The Trading Show London: ReFLEX CES Showcases Ultra low-latency FPGA network accelerator cards

Booth 17, March 22-23, 2016, London, England

London, England, The Trading Show London, March 17, 2016 - ReFLEX CES, a leading European-based provider of custom embedded and complex systems, will showcase its expertise in the design and manufacture of complex Ultra low-latency FPGA network accelerator cards at The Trading Show London 2016. Highlights of the stand include Networking & Processing FPGA boards, Instant-DevKits and OpenCL demos.

The Trading Show London, provides the perfect platform for ReFLEX CES to reveal how it is further extending its proven position in FPGA-based solutions for the Finance industry:

New FPGA boards

ReFLEX CES is taking advantage of this exhibition to announce a new Low Profile Arria10 GX FPGA board which complements the existing high-Performance Computing and Finance solutions.

Instant-DevKit Solutions

See also the Attila and Alaric Instant-DevKits offering developers an out-of-the box design solution that combines a compact hardware platform with an efficient, intuitive software environment. The DevKit's unique install and graphical user interface enable an immediate start, and its reference designs enable fast turn-around for short, secure developments.

OpenCL

REFLEX CES will also demonstrate a High Performance Computing (HPC) OpenCL BSP (Board Support Package) based on its Attila Arria 10 GX Instant-DevKit. This solution is a ready to use PCIe Arria 10 GX/SoC FPGA-based hardware accelerator and offers users, a quick way of implementing complex parallel algorithms in FPGAs. The Attila HPC OpenCL BSP abstracts the hardware layer from the programmer and allows them, with little or no FPGA development skills, to quickly and easily implement his algorithms on a 100% FPGA accelerator target.

High-speed FPGA boards catalog

See also the FPGA accelerator network processing boards namely the XpressGX5LP-SE, XpressGX5LP-QE and XpressV7LP product lines.

The combination of PCI Express, 10G Ethernet, and memory interfaces on highly integrated cards make the perfect production-ready programmable solutions for high performance, ultra low latency network-based computing. ReFLEX CES's use of leading-edge FPGAs from manufacturers Altera Corp. (ALTR) and Xilinx, Inc. (XLNX) provides assurance of quality and reliability. The Altera Arria® & Stratix® and Xilinx Virtex® families of FPGA deliver the highest density, the highest performance, and the lowest power. Leveraging the benefits of leading edge process technologies and proven transceiver and memory interface technology, these FPGAs provides an unprecedented level of system bandwidth with superior signal integrity.

Committed to ambitious plans for growth, ReFLEX CES is actively hiring engineers in hardware, software, firmware, CAD, mechanics and complete systems development. ReFLEX CES achieved a growth of more than 20% in 2015 to reach revenue of 12 million Euros.

Interviews

To schedule a meeting with ReFLEX CES, please email kmartin@reflexces.com.

About Reflex CES

ReFLEX CES entered the HPC world 5 years ago and has been supporting Finance players with their FPGA network acceleration cards for the last four years. Their track record is already consistent and ReFLEX FPGA boards are considered as references. Recognized for its expertise in high-speed applications and low-latency hardware, ReFLEX CES has become a leading partner for the Finance market and our technology is deployed at numerous financial institutions worldwide, including banks, hedge funds, and exchanges.

ReFLEX CES simplifies the adoption of FPGA technology with its leading edge FPGA-based ultra low latency programmable network platforms. ReFLEX CES FPGA network platforms enable sub-microsecond latency market data processing and order execution and enable orders of magnitude superior performance for algorithmic trading, including options pricing and risk management, over conventional software-based and hybrid approaches.

For more information, visit <http://www.reflexces.com>

